

Team Member 1

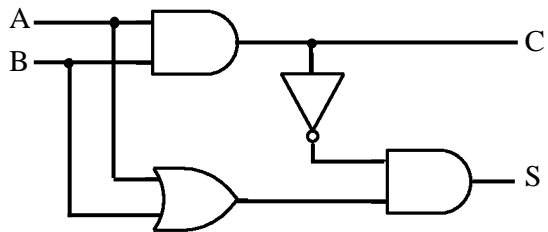


Fig. 1 Adder circuit

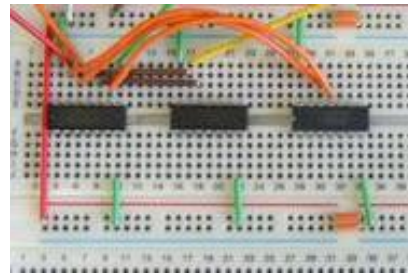


Fig. 2 Photograph of the test circuit

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 1. Truth table

Team Member 2

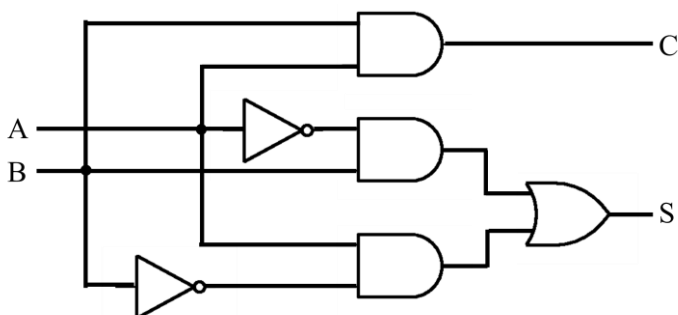


Fig. 1 Adder circuit

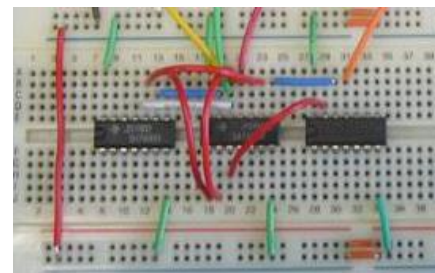


Fig. 2 Photograph of the test circuit

A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 1. Truth table

Team Member 3

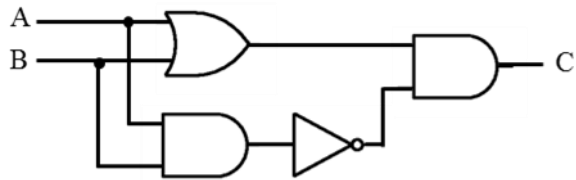


Fig. 1 XOR circuit

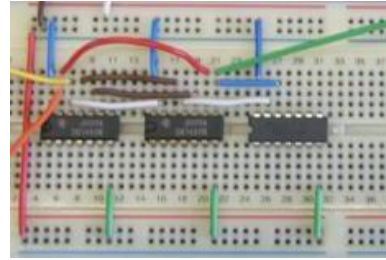


Fig. 2 Photograph of the test circuit

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Table 1. Truth table

Team Member 4

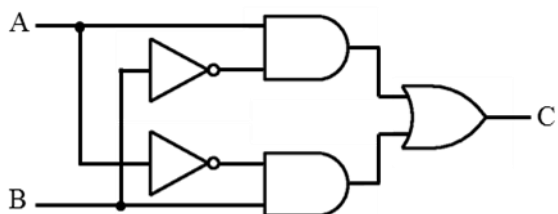


Fig. 1 XOR circuit

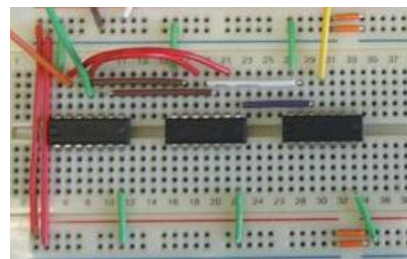


Fig. 2 Photograph of the test circuit

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Table 1. Truth table